FAIRCHILD SEMICONDUCTOR®

June 2008

FXL2SD106
Low Voltage Dual Supply 6-Bit SD Interface Voltage Translator with Configurable Voltage Supplies and Signal Levels, 3-State Outputs, and Auto Direction Sensing

Features

- Bi-directional interface between two levels from 1.1V to 3.6V
- Fully configurable: Inputs and outputs track V_{CC} level
- Non-preferential power-up; either VCC may be powered-up first
- Outputs remain in 3-state until active V_{CC} level is reached
- Outputs switch to 3-state if either V_{CC} is at GND.
- Power off protection
- Bushold on data inputs eliminates the need for SDIO pull-up resistors
- Control input (OE and CLK IN) are referenced to V_{CCA} voltage
- Packaged in 16-terminal DQFN (2.5mm x 3.5mm)
- Direction control not needed
- 80 Mbps throughput when translating between 1.8V and 2.5V
- ESD protection exceeds:
  - 12kV HBM (B port I/O to GND) (per JESD22-A114 & Mil Std 883e 3015.7)
  - 8kV HBM (A port I/O to GND) (per JESD22-A114 & Mil Std 883e 3015.7)
  - 1kV CDM (per ESD STM 5.3)

General Description

The FXL2SD106 is a configurable dual-voltage-supply translator designed for both uni-directional and bi-directional voltage translation between two logic levels. The device allows translation between voltages as high as 3.6V to as low as 1.1V. The A port tracks the V_{CCA} level, and the B port tracks the V_{CCB} level. This allows for bi-directional voltage translation over a variety of voltage levels: 1.2V, 1.5V, 1.8V, 2.5V and 3.3V.

The FXL2SD106 is specifically designed as a translator to interface with the SDIO standard. I/O capacitance is managed to meet the SD maximum capacitance specification. The B side ESD performance allows interface as an external card and the part can handle 80 Mbps throughput when translating between 1.8V and 2.5V.

The device remains in 3-state until both V_{CC}s reach active levels allowing either V_{CC} to be powered-up first. Internal power down control circuits place the device in 3-state if either VCC is removed.

The OE input, when low, disables both the A and B ports by placing them in a 3-state condition. The FXL2SD106 is designed so that both control pins (OE and CLK IN) are supplied by V_{CCA}.

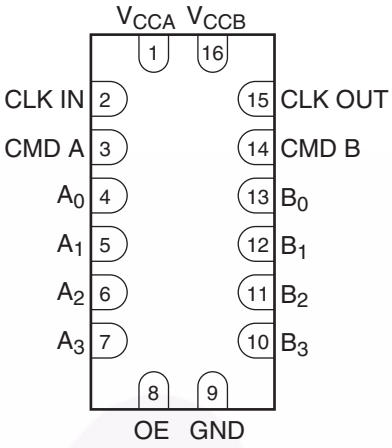
The device senses an input signal on A or B port automatically. The input signal is transferred to the other port.

Ordering Information

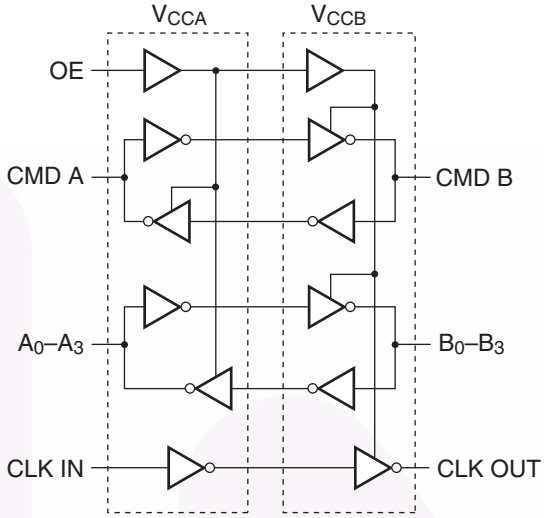
Order Number	Package Number	Package Description
FXL2SD106BQX	MLP16E	16-Terminal Depopulated Quad Very-Thin Flat Pack, No Leads (DQFN), JEDEC MO-241, 2.5mm x 3.5mm

All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram



Functional Diagram



Pin Description

Number	Name	Description
1	V_{CCA}	A Side Power Supply
2	CLK IN	A Side Input
3	CMD A	A Side Inputs or 3-State Outputs
4–7	A_0–A_3	
8	OE	Output Enable Input
9	GND	
10–13	B_3–B_0	B Side Inputs or 3-State Outputs
14	CMD B	
15	CLK OUT	3-State Output
16	V_{CCB}	B Side Power Supply

Function Table

Control	
OE	Outputs
L	3-State
H	Normal Operation

H = HIGH Logic Level

L = LOW Logic Level

Power-Up/Power-Down Sequencing

FXL translators offer an advantage in that either Vcc may be powered up first. This benefit derives from the chip design. When either V_{CC} is at 0 volts, outputs are in a high-impedance state. The control input (OE) is designed to track the VccA supply. A pull-down resistor tying OE to GND should be used to ensure that bus contention, excessive currents, or oscillations do not occur during power-up/power-down. The size of the pull-down resistor is based upon the current-sinking capability of the device driving the OE pin.

The recommended power-up sequence is the following:

1. Apply power to the first V_{CC}.
2. Apply power to the second V_{CC}.
3. Drive the OE input high to enable the device.

The recommended power-down sequence is the following:

1. Drive OE input low to disable the device.
2. Remove power from either V_{CC}.
3. Remove power from other V_{CC}.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CCA}, V_{CCB}	Supply Voltage	–0.5V to +4.6V
V_I	DC Input Voltage	
	I/O Port A	–0.5V to +4.6V
	I/O Port B	–0.5V to +4.6V
	Control Inputs (OE, CLK IN)	–0.5V to +4.6V
V_O	Output Voltage(1)	
	Outputs 3-STATE	–0.5V to +4.6V
	Outputs Active (A_n, CMD A)	–0.5V to V_{CCA} + 0.5V
	Outputs Active (B_n, CMD B, CLK OUT)	–0.5V to V_{CCB} + 0.5V
I_{IK}	DC Input Diode Current @ V_I < 0V	–50mA
I_{OK}	DC Output Diode Current @	
	V_O < 0V	–50mA
	V_O > V_{CC}	+50mA
I_{OH} / I_{OL}	DC Output Source/Sink Current	–50mA / +50mA
I_{CC}	DC V_{CC} or Ground Current per Supply Pin	±100mA
T_{STG}	Storage Temperature Range	–65°C to +150°C

Note:

1. I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions(2)

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CCA} or V_{CCB}	Power Supply Operating	1.1V to 3.6V
	Input Voltage	
	Port A	0.0V to 3.6V
	Port B	0.0V to 3.6V
	Control Inputs (OE, CLK IN)	0.0V to V_{CCA}
	Dynamic Output Current in I_{OH}/I_{OL} with V_{CC} @	
	3.0V to 3.6V	±18.0mA
	2.3V to 2.7V	±11.8mA
	1.65V to 1.95V	±7.4mA
	1.4V to 1.65V	±5.0mA
	1.1V to 1.4V	±2.6mA
	Static Output Current I_{OH}/I_{OL} with V_{CC} @ 1.1V to 3.6V	±20.0µA
T_A	Free Air Operating Temperature	–40°C to +85°C
$\Delta t / \Delta V$	Maximum Input Edge Rate $V_{CCA/B}$ = 1.1V to 3.6V	10ns/V

Note:

2. All unused inputs and I/O pins must be held at V_{CCI} or GND.

DC Electrical Characteristics (T_A = –40°C to +85°C)

Symbol	Parameter	V_{CCA} (V)	V_{CCB} (V)	Conditions	Min.	Typ.	Max.	Units
V_{IH}	High Level Input Voltage	1.4–3.6	1.1–3.6	Data inputs An, CMD A, Control inputs CLK IN, OE	0.6 x V_{CCA}			V
		1.1–1.4	1.1–3.6		0.9 x V_{CCA}			
		1.1–3.6	1.4–3.6	Data inputs Bn, CMD B	0.6 x V_{CCB}			
		1.1–3.6	1.1–1.4		0.9 x V_{CCB}			
V_{IL}	Low Level Input Voltage	1.4–3.6	1.1–3.6	Data inputs An, CMD A, Control inputs CLK IN, OE			0.35 x V_{CCA}	V
		1.1 –1.4	1.1–3.6				0.1 x V_{CCA}	
		1.1–3.6	1.4–3.6	Data inputs Bn, CMD B			0.35 x V_{CCB}	
		1.1–3.6	1.1–1.4				0.1 x V_{CCB}	
V_{OH}[3]	High Level Output Voltage	1.65–3.6	1.1–3.6	Data outputs An, CMD A, I_{HOLD} = –20µA	0.75 x V_{CCA}			V
		1.1–1.4	1.1–3.6			0.8		
		1.1–3.6	1.65–3.6	Data outputs Bn, CMD B, I_{HOLD} = –20µA	0.75 x V_{CCB}			
		1.1–3.6	1.1–1.4			0.8		
V_{OL}[3]	Low Level Output Voltage	1.65–3.6	1.1–3.6	Data outputs An, CMD A, I_{HOLD} = 20µA			0.2 x V_{CCA}	V
		1.1–1.4	1.1–3.6			0.3		
		1.1–3.6	1.65–3.6	Data outputs Bn, CMD B, I_{HOLD} = 20µA			0.2 x V_{CCB}	
		1.1–3.6	1.1–1.4			0.3		
$I_{I(ODH)}$[4]	Bushold Input Overdrive High Current	3.6	3.6	Data inputs An, CMD A, Bn, CMD B	450			µA
		2.7	2.7		300			
		1.95	1.95		200			
		1.6	1.6		120			
		1.4	1.4		80			
$I_{I(ODL)}$[5]	Bushold Input Overdrive Low Current	3.6	3.6	Data inputs An, CMD A, Bn, CMD B	-450			µA
		2.7	2.7		-300			
		1.95	1.95		-200			
		1.6	1.6		-120			
		1.4	1.4		-80			
I_I	Input Leakage Current	1.1–3.6	3.6	Control inputs OE, CLK IN, V_I = V_{CCA} or GND			±1.0	µA
I_{OFF}	Power Off Leakage Current	0	3.6	An, CMD A, V_O = 0V to 3.6V			±2.0	µA
		3.6	0	Bn, CMD B, CLK OUT, V_O = 0V to 3.6V			±2.0	
I_{OZ}[6]	3-State Output Leakage	3.6	3.6	An, CMD A, Bn, CMD B, CLK OUT, V_O = 0V or 3.6V, OE = V_{IL}			±2.0	µA
		3.6	0	An, CMD A, V_O = 0V or 3.6V, OE = Don't Care			±2.0	
		0	3.6	Bn, CMD B, CLK OUT, V_O = 0V or 3.6V, OE = Don't Care			±2.0	
$I_{CCA/B}$[7][8]	Quiescent Supply Current	1.1–3.6	1.1–3.6	V_I = V_{CCI} or GND, I_O = 0			5.0	µA
I_{CCZ}[7]	Quiescent Supply Current	1.1–3.6	1.1–3.6	V_I = V_{CCI} or GND, I_O = 0, OE = V_{IL}			5.0	µA

DC Electrical Characteristics (T_A = –40°C to +85°C) (Continued)

Symbol	Parameter	V_{CCA} (V)	V_{CCB} (V)	Conditions	Min.	Typ.	Max.	Units
I_{CCA}[7]	Quiescent Supply Current	0	1.1–3.6	$V_I = V_{CCB}$ or GND; $I_O = 0$			-2.0	µA
		1.1–3.6	0	$V_I = V_{CCA}$ or GND; $I_O = 0$			2.0	
I_{CCB}[7]	Quiescent Supply Current	1.1–3.6	0	VI = V_{CCB} or GND; IO = 0			-2.0	µA
		0	1.1–3.6	VI = V_{CCA} or GND; IO = 0			2.0	

Notes:

3. This is the output voltage for static conditions. Dynamic drive specifications are given in “Dynamic Output Electrical Characteristics.”
4. An external driver must source at least the specified current to switch LOW-to-HIGH.
5. An external driver must source at least the specified current to switch HIGH-to-LOW.
6. “Don’t Care” indicates any valid logic level.
7. V_{CCI} is the V_{CC} associated with the input side.
8. Reflects current per supply, V_{CCA} or V_{CCB}.

Dynamic Output Electrical Characteristics[9]

A Port (An, CMD A)

Output Load: C_L = 15pF, $R_L \geq 1M\Omega$ ($C_{I/O}$ = 5pF)

		T_A = -40°C to +85°C, V_{CCA} =									
		3.0V to 3.6V		2.3V to 2.7V		1.65V to 1.95V		1.4V to 1.6V		1.1V to 1.3V	
Symbol	Parameter	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Units
t_{rise}[10]	Output Rise Time A port		3.0		3.5		4.0		5.0	7.5	ns
t_{fall}[11]	Output Fall Time A port		3.0		3.5		4.0		5.0	7.5	ns
I_{OHD}[10]	Dynamic Output Current High	-18.0		-11.8		-7.4		-5.0		-2.6	mA
I_{OLD}[11]	Dynamic Output Current Low	+18.0		+11.8		+7.4		+5.0		+2.6	mA

B Port (Bn, CMD B, CLK OUT)

Output Load: C_L = 15pF, $R_L \geq 1M\Omega$ ($C_{I/O}$ = 15pF)

		T_A = -40°C to +85°C, V_{CCB} =									
		3.0V to 3.6V		2.3V to 2.7V		1.65V to 1.95V		1.4V to 1.6V		1.1V to 1.3V	
Symbol	Parameter	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Units
t_{rise}[10]	Output Rise Time A port		3.0		3.5		4.0		5.0	7.5	ns
t_{fall}[11]	Output Fall Time A port		3.0		3.5		4.0		5.0	7.5	ns
I_{OHD}[10]	Dynamic Output Current High	-18.0		-11.8		-7.4		-5.0		-2.6	mA
I_{OLD}[11]	Dynamic Output Current Low	+18.0		+11.8		+7.4		+5.0		+2.6	mA

Notes:

9. Dynamic Output Characteristics are guaranteed but not tested.
10. See Figure 5.
11. See Figure 6.

AC Characteristics

V_{CCA} = 3.0V to 3.6V

Symbol	Parameter	T_A = -40°C to +85°C, V_{CCB} =									Units
		3.0V–3.6V		2.3V–2.7V		1.65V–1.95V		1.4V–1.6V		1.1V–1.3V	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Typ.	
t_{PLH}, t_{PHL}	A to B	0.2	3.5	0.3	3.9	0.5	5.4	0.6	6.8	22.0	ns
	B to A	0.2	3.5	0.2	3.8	0.3	5.0	0.5	6.0	15.0	ns
t_{PLH}, t_{PHL}	CLK IN to CLK OUT		3.0		3.5		4.5		6.0	15.0	ns
t_{PZL}, t_{PZH}	OE to A, OE to B		1.7		1.7		1.7		1.7	1.7	µs
t_{skew}(12)	A Port, B Port		0.5		0.5		0.5		1.0	1.0	ns

V_{CCA} = 2.3V to 2.7V

Symbol	Parameter	T_A = -40°C to +85°C, V_{CCB} =									Units
		3.0V–3.6V		2.3V–2.7V		1.65V–1.95V		1.4V–1.6V		1.1V–1.3V	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Typ.	
t_{PLH}, t_{PHL}	A to B	0.2	3.8	0.4	4.2	0.5	5.6	0.8	6.9	22.0	ns
	B to A	0.3	3.9	0.4	4.2	0.5	5.5	0.5	6.5	15.0	ns
t_{PLH}, t_{PHL}	CLK IN to CLK OUT		3.5		4.0		4.5		6.5	15.0	ns
t_{PZL}, t_{PZH}	OE to A, OE to B		1.7		1.7		1.7		1.7	1.7	µs
t_{skew}(12)	A Port, B Port		0.5		0.5		0.5		1.0	1.0	ns

V_{CCA} = 1.65V to 1.95V

Symbol	Parameter	T_A = -40°C to +85°C, V_{CCB} =									Units
		3.0V–3.6V		2.3V–2.7V		1.65V–1.95V		1.4V–1.6V		1.1V–1.3V	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Typ.	
t_{PLH}, t_{PHL}	A to B	0.3	5.0	0.5	5.5	0.8	6.7	0.9	7.5	22.0	ns
	B to A	0.5	5.4	0.5	5.6	0.8	6.7	1.0	7.0	15.0	ns
t_{PLH}, t_{PHL}	CLK IN to CLK OUT		4.5		4.5		6.3		6.7	15.0	ns
t_{PZL}, t_{PZH}	OE to A, OE to B		1.7		1.7		1.7		1.7	1.7	µs
t_{skew}(12)	A Port, B Port		0.5		0.5		0.5		1.0	1.0	ns

V_{CCA} = 1.4V to 1.6V

Symbol	Parameter	T_A = -40°C to +85°C, V_{CCB} =									Units
		3.0V–3.6V		2.3V–2.7V		1.65V–1.95V		1.4V–1.6V		1.1V–1.3V	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Typ.	
t_{PLH}, t_{PHL}	A to B	0.5	6.0	0.5	6.5	1.0	7.0	1.0	8.5	22.0	ns
	B to A	0.6	6.8	0.8	6.9	0.9	7.5	1.0	8.5	15.0	ns
t_{PLH}, t_{PHL}	CLK IN to CLK OUT		6.0		6.5		6.7		8.5	15.0	ns
t_{PZL}, t_{PZH}	OE to A, OE to B		1.7		1.7		1.7		1.7	1.7	µs
t_{skew}(12)	A Port, B Port		1.0		1.0		1.0		1.0	1.0	ns

Note:

12. Skew is the variation of propagation delay between output signals and applies only to output signals on the same port (An, CMD A or Bn, CMD B) and switching with the same polarity (Low-to-High or High-to-Low). See Figure 8.

Max Data Rate[13][14]

V_{CCA}	T_A = -40°C to +85°C, V_{CCB} =					Units
	3.0V to 3.6V	2.3V to 2.7V	1.65V to 1.95V	1.4V to 1.6V	1.1V to 1.3V	
	Min.	Min.	Min.	Min.	Typ.	
V_{CCA} = 3.0V to 3.6V	100	100	80	60	20	Mbps
V_{CCA} = 2.3V to 2.7V	100	100	80	60	20	Mbps
V_{CCA} =1.65V to 1.95V	80	80	60	40	20	Mbps
V_{CCA} = 1.4V to 1.6V	60	60	40	40	20	Mbps
	Typ.	Typ.	Typ.	Typ.	Typ.	
V_{CCA} = 1.1V to 1.3V	20	20	20	20	20	Mbps

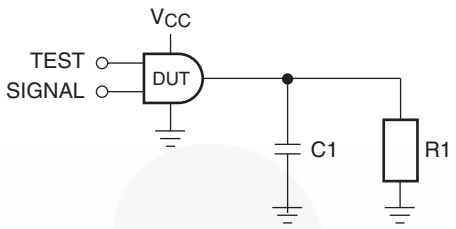
Note:

13. Max Data Rate is guaranteed but not tested.

14. Max Data Rate is specified in megabits per second. See Figure 7. It is equivalent to two times the F-toggle frequency, specified in megahertz. For example, 100 Mbps is equivalent to 50 MHz.

Capacitance

Symbol	Parameter		Conditions	T_A = +25°C Typical	Units
Cin	Input Capacitance, Control pin (OE, CLK IN)		VccA = VccB = GND	4	pF
Ci/o	Input/Output Capacitance	An, CMD A	VccA = VccB = 3.3V, OE = VccA	5	pF
		Bn, CMD B, CLK OUT		6	
Cpd	Power Dissipation Capacitance		VccA = VccB = 3.3V, Vi = 0V or Vcc, f = 10MHz	25	pF

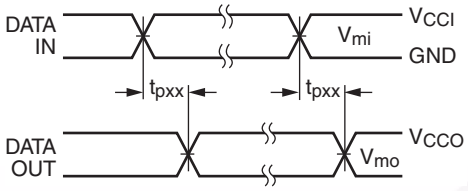


Test	Input Signal	Output Enable Control
t_{PLH}, t_{PHL}	Data Pulses	V_{CCA}
t_{PZL}	0V	Low to High Switch
t_{PZH}	V_{CCI}	Low to High Switch

Figure 1. AC Test Circuit

AC Load Table

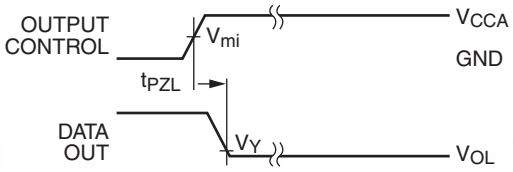
V_{CCO}	Cl	Rl
1.2V ± 0.1V	15pF	1MΩ
1.5V ± 0.1V	15pF	1MΩ
1.8V ± 0.15V	15pF	1MΩ
2.5V ± 0.2V	15pF	1MΩ
3.3 ± 0.3V	15pF	1MΩ



Input $t_R = t_F$ = 2.0ns, 10% to 90%

Input $t_R = t_F$ = 2.5ns, 10% to 90%, @ Vi = 3.0V to 3.6V only

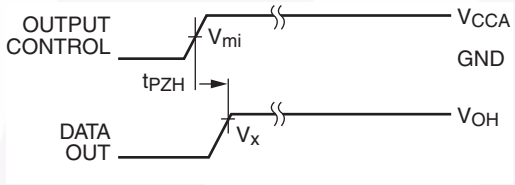
Figure 2. Waveform for Inverting and Non-inverting Functions



Input $t_R = t_F$ = 2.0ns, 10% to 90%

Input $t_R = t_F$ = 2.5ns, 10% to 90%, @ Vi = 3.0V to 3.6V only

Figure 3. 3-STATE Output Low Enable Time for Low Voltage Logic



Input $t_R = t_F$ = 2.0ns, 10% to 90%

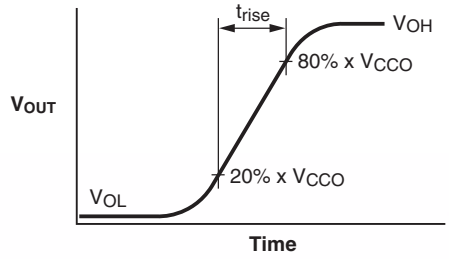
Input $t_R = t_F$ = 2.5ns, 10% to 90%, @ Vi = 3.0V to 3.6V only

Figure 4. 3-STATE Output High Enable Time for Low Voltage Logic

Symbol	Vcc
Vmi(15)	V_{CCI} / 2
Vmo	V_{CCO} / 2
VX	0.9 x V_{CCO}
VY	0.1 x V_{CCO}

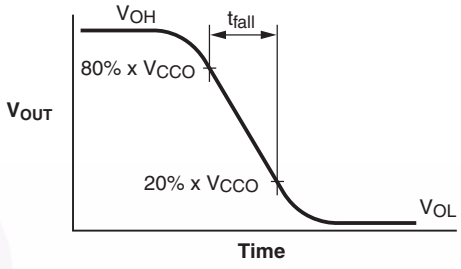
Note:

15. $V_{CCI} = V_{CCA}$ for control pin OE or Vmi = (V_{CCA} / 2).



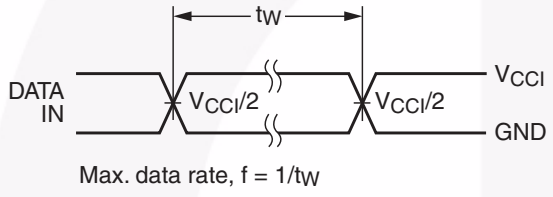
$$I_{OHD} \approx (C_L + C_{I/O}) \times \frac{\Delta V_{OUT}}{\Delta t} = (C_L + C_{I/O}) \times \frac{(20\% - 80\%) \times V_{CCO}}{t_{RISE}}$$

Figure 5. Active Output Rise Time and Dynamic Output Current High



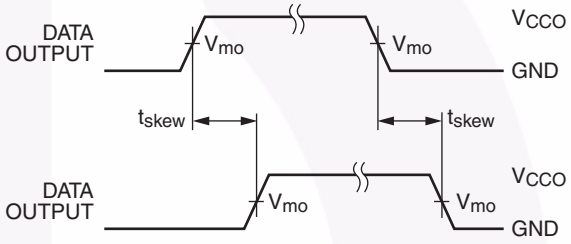
$$I_{OLD} \approx (C_L + C_{I/O}) \times \frac{\Delta V_{OUT}}{\Delta t} = (C_L + C_{I/O}) \times \frac{(80\% - 20\%) \times V_{CCO}}{t_{FALL}}$$

Figure 6. Active Output Fall Time and Dynamic Output Current Low



Max. data rate, f = $1/t_W$

Figure 7. Maximum Data Rate



$t_{skew} = (t_{pHLmax} - t_{pHLmin})$ or $(t_{pLHmax} - t_{pLHmin})$

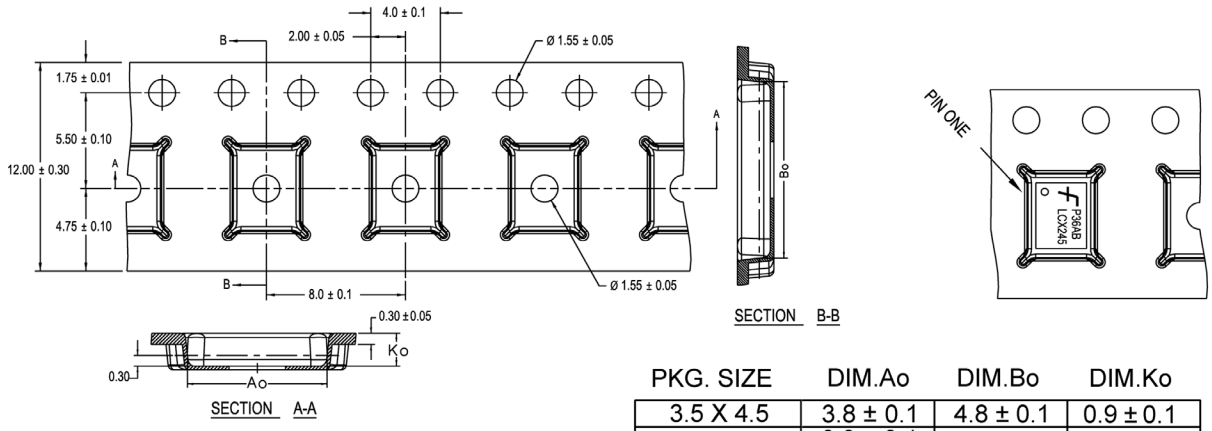
Figure 8. Output Skew Time

Tape and Reel Specification

Tape Format for DQFN 10

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
BQX	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	2500/3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

Tape Dimensions millimeters



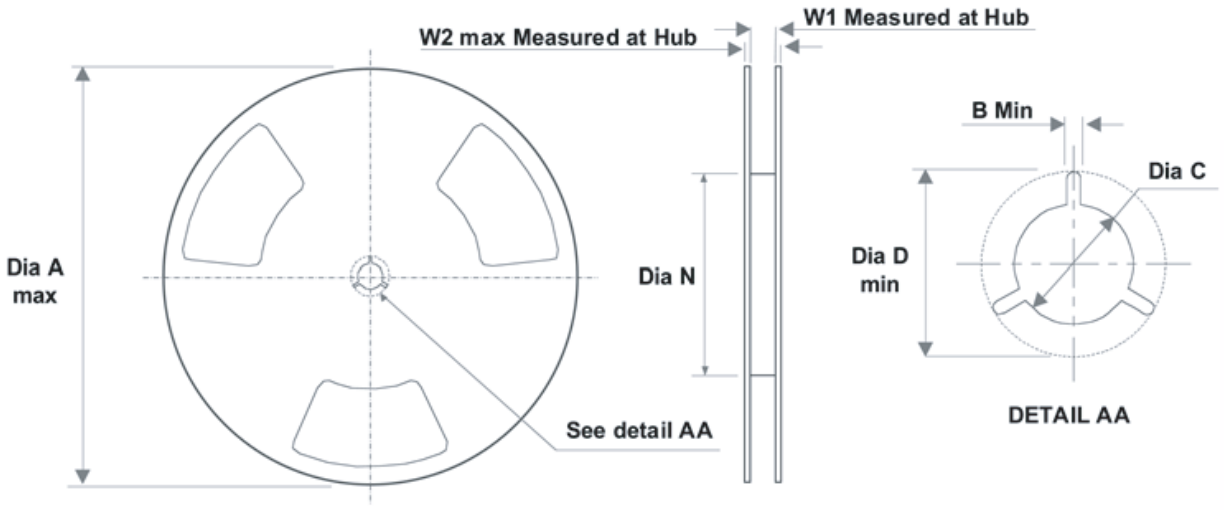
PKG. SIZE	DIM.Ao	DIM.Bo	DIM.Ko
3.5 X 4.5	3.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
3.0 X 3.0	3.3 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 4.5	2.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
2.5 X 3.5	2.8 ± 0.1	3.8 ± 0.1	0.9 ± 0.1
2.5 X 3.0	2.8 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 2.5	2.8 ± 0.1	2.8 ± 0.1	0.9 ± 0.1

DIMENSIONS ARE IN MILLIMETERS

NOTES: unless otherwise specified

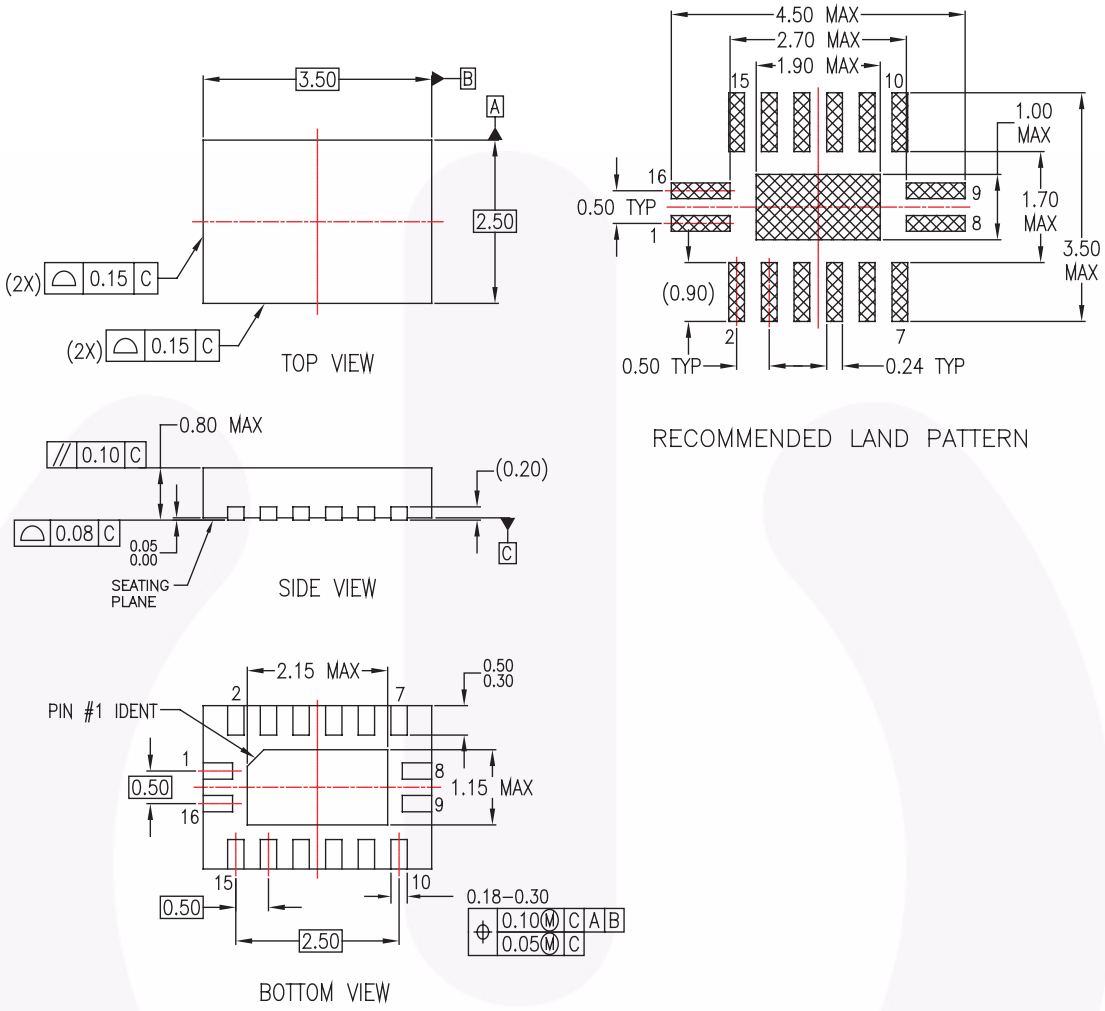
1. Cummulative pitch for feeding holes and cavities (chip pockets) not to exceed 0.008[0.20] over 10 pitch span.
2. Smallest allowable bending radius.
3. Thru hole inside cavity is centered within cavity.
4. Tolerance is ±0.002[0.05] for these dimensions on all 12mm tapes.
5. Ao and Bo measured on a plane 0.120[0.30] above the bottom of the pocket.
6. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket. Not pocket hole.
8. Controlling dimension is millimeter. Diemension in inches rounded.

Reel Dimensions inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2
12mm	13.0 (330)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	7.008 (178)	0.488 (12.4)	0.724 (18.4)

Physical Dimensions



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO–241, VARIATION AB
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP16ErevA

Figure 9. 6-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241 2.5mm x 3.5mm

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